LTM-10A
User's Guide

Revision 4

ECHELON®
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078-0132-01D

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Contents

1

LTM-10A Overview

The LTM-10 family of products, which includes the LTM-10A Flash Control Module, the LTM-10 Motherboard, and the LTM-10A Platform provides a modular family of easy-to-use tools for rapidly developing LONWORKS® devices. The LTM-10A module contains a Neuron® 3150® Chip, flash memory, RAM, crystal, and reset circuitry, thereby forming the basic building block for a LONWORKS device. The LTM-10 Motherboard contains all the necessary components to allow the use of the LTM-10A module on a LONWORKS network including support for an SMX transceiver, a power supply, reset and service switches, and status indicators. The LTM-10A platform combines the LTM-10A module, the LTM-10 Motherboard, and an SMX transceiver in an enclosure. The LTM-10A platform is shipped as part of the NodeBuilder® Development Tool; and the LTM-10A platform, LTM-10A module, and LTM-10 Motherboard also are available as stand-alone products.

LTM-10A Flash Control Module

The LTM-10A module includes a flash memory with Neuron Chip firmware version 121 and a Microprocessor Interface Program (MIP) image. The MIP image is based on the MIP/P50 firmware and can be used to interface the LTM-10A module with an external host processor.

The version 121 firmware manages four memory maps that enable you to allocate the LTM-10A 64Kbyte flash memory and the 32Kbyte RAM to the available 56Kbyte address space on the LTM-10A module. The LTM-10A firmware automatically selects the appropriate memory map when an image is downloaded to the LTM-10A module. The memory maps are described in Chapter 4. Figure 1.1 shows a photograph of the LTM-10A module.

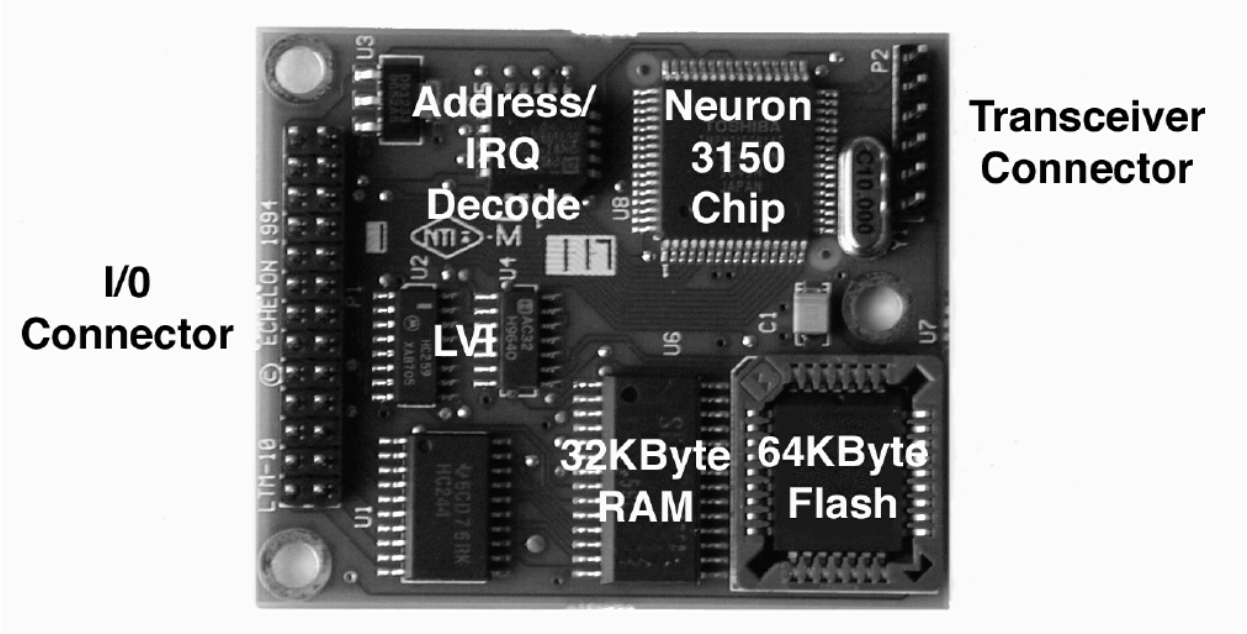


Figure 1.1 LTM-10A module

The module also includes the MIP/P50 firmware which can be used to interface the on-board Neuron Chip to an external host processor.

LTM-10 Motherboard

The LTM-10 Motherboard enables the user to easily interface an LTM-10A module to an SMX transceiver of their choice. SMX transceivers are available for different media from Echelon and other third party sources. The LTM-10 Motherboard also provides a +5VDC supply for the LTM-10A Flash Control Module and the on-board SMX transceiver, a service LED and switch, a reset LED and switch, and an LED and a switch for application development. A connector is provided which enables the Neuron Chip's I/O pins to be brought out for interfacing to external I/O or a host processor. The motherboard contains a connector for the user to provide regulated +5VDC input for use with transceivers and external I/O that require more than the

500mA provided by the LTM-10 power supply. Figure 1.2 shows the block diagram of the LTM-10 Motherboard.

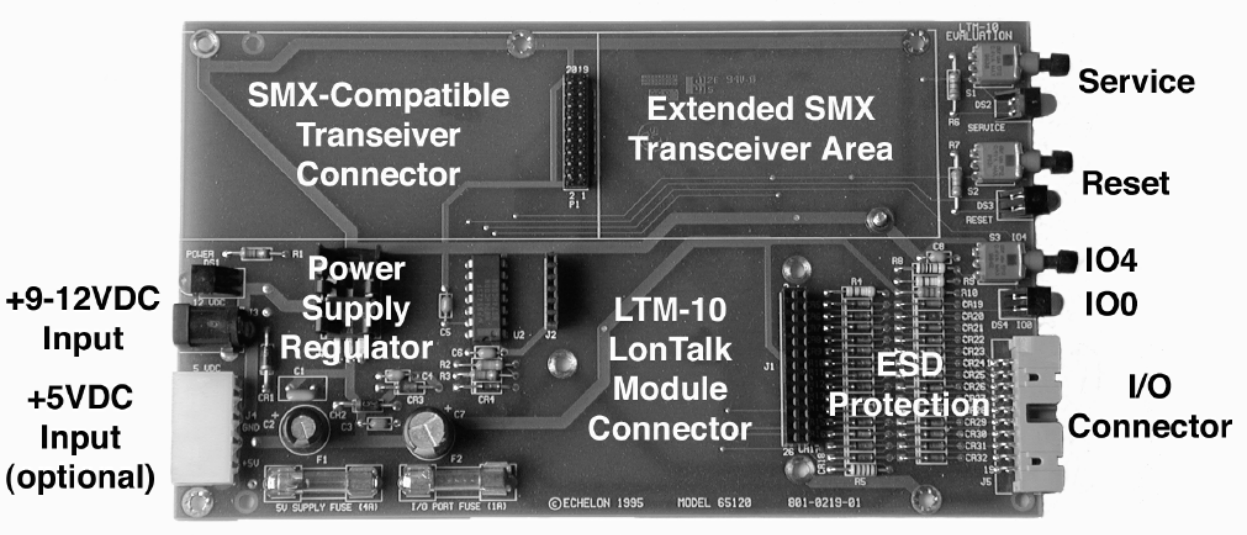


Figure 1.2 LTM-10 Motherboard Block Diagram (size not to scale)

LTM-10A Platform

The LTM-10A platform implements a complete LONWORKS device. This is accomplished by integrating the LTM-10 Motherboard, the LTM-10A flash control module, a wall-mount power supply, and an SMX transceiver. The complete modular assembly is enclosed to allow for easy portability and protection. Figure 1.3 shows a photograph of the LTM-10A platform.

Figure 1.3 LTM-10A Platform

LTM-10A Applications

A LONWORKS device can be either Neuron Chip-hosted or host-based. A Neuron Chip-hosted device uses a Neuron Chip as its sole processor. The Neuron Chip is responsible for running the user application as well as the LonTalk protocol for communicating on the LONWORKS network. As an OEM building block, the LTM-10A module is designed to be easily integrated into LONWORKS products. On-board flash memory permits the user application program to reside in non-volatile memory, and thus be changed over the network at any time. On-board RAM memory can be used by the user application program for program data and additional communication buffers. Additionally, the on-board RAM may be used in a development environment to store the application program, thereby reducing write cycles to the flash memory. Refer to the NodeBuilder or LonBuilder® user guides for more information on developing Neuron Chip hosted LONWORKS devices. Figure 1.4 shows the architecture of a Neuron Chip-hosted device using the LTM-10A module.

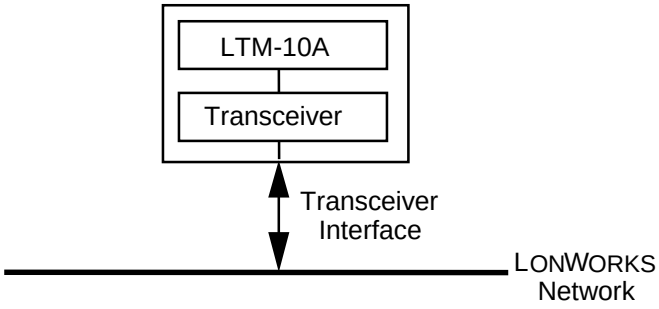


Figure 1.4 Neuron Chip-Hosted Device Architecture

Host-based devices can be used for applications that require more processing power, memory, or I/O capability than provided by the Neuron Chip. In this case, the Neuron Chip becomes a communication processor. The application processing occurs on an external host processor. Host applications can also be used to interface an existing application to a LONWORKS network.

You can create a host-based device using a ShortStack™ Micro Server or a Microprocessor Interface Program (MIP). The ShortStack Micro Server provides the easiest to use interface with the least overhead required on a host. You can download the ShortStack firmware and documentation from www.echelon.com/shortstack.

The LTM-10A module contains the Microprocessor Interface Program (MIP) version P50 that also may be used in developing a host-based device. The MIP/P50 is included as part of the system image on the LTM-10A Flash Control Module, and is invoked by the application programmer through the use of Neuron C code.

Figure 1.5 shows the architecture of a host-based device using the LTM-10A module.

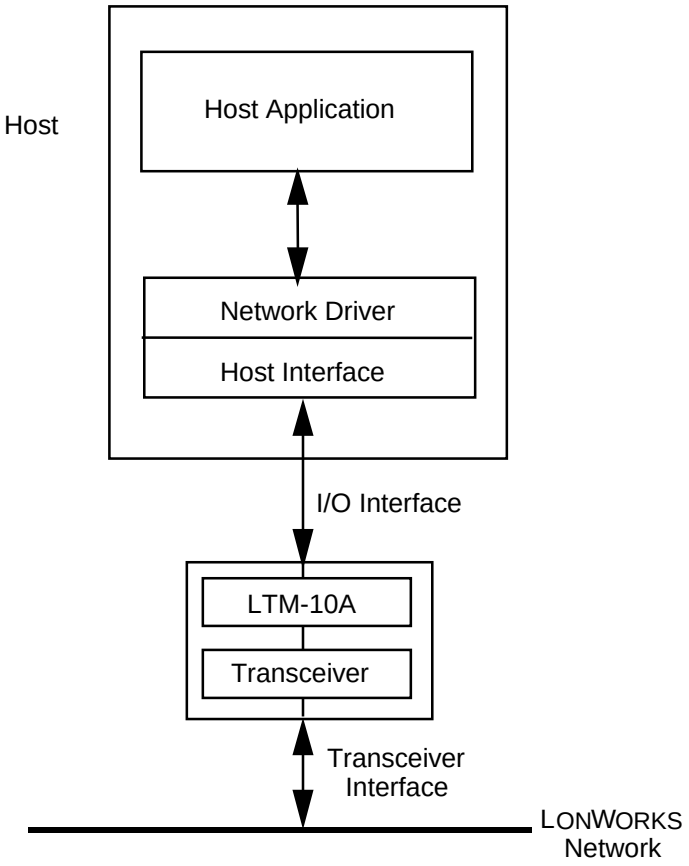


Figure 1.5 Host-based Device Architecture

Refer to the *Microprocessor Interface Program User's Guide* and the *Host Application Programmer's Guide* for more information on the MIP and the requirements for writing a host application when using the MIP.

Audience

The *LTM-10A User's Guide* provides specifications and user instructions for customers who have purchased the LTM-10A module.

Content

This manual provides an overview of the LTM-10A flash control module, LTM-10 Motherboard, LTM-10A platform, and LTM-10A applications.

Chapter 2 describes the process of getting started with the LTM-10A platform.

Chapter 3 provides information for designing in the LTM-10A flash control module.

Chapter 4 discusses the steps necessary for programming the LTM-10A module.

Chapter 5 explains the use of the LTM-10A module as a network interface.

Naming Conventions

This guide uses the following conventions:

A leading tilde or a trailing minus sign indicates asserted-low signals. For example: ~RESET and RESET- mean reset asserted-low.

When ~RESET or RESET- is voltage low, it is ON. When it is voltage high, it is OFF.

Code fragments and examples appear in `Courier` font.

Related Documentation

The following is a list of documents available from Echelon that provide additional information related to custom nodes. You can download PDF versions of these manuals from the Echelon web site at www.echelon.com/products.

- *FT 3120® and FT 3150® Smart Transceivers Databook*. Describes the memory, I/O, and communications ports of the Neuron Chip, together with the support circuitry required for clock, reset, and service functions. Pin assignment, pad layout, and electrical and environmental specifications are also provided.
- *LonBuilder User's Guide*. Describes the process of software and hardware prototyping of custom nodes using the LonBuilder tools. Chapter 7 includes a detailed discussion of custom device development.
- *NodeBuilder User's Guide*. Describes the process of software and hardware prototyping of custom devices using the NodeBuilder tool.
- *LonBuilder Hardware Guide*. Describes the LonBuilder hardware. Chapter 2 describes the hardware products that can be used for prototyping and developing custom devices. These products include the LONWORKS Module Application Interface which is used to debug custom devices based on LONWORKS control modules including the LTM-10A module.
- *Neuron C Programmer's Guide*. Provides an overview of the Neuron C programming language.
- *Neuron C Reference Guide*. Provides reference information on the functions and features available within Neuron C.
- *LONWORKS Host Application Programmer's Guide*. Describes the process of developing application programs that run on host processors other than the Neuron Chip.
- *LONMARK® Layers 1-6 Interoperability Guidelines*. Provides guidelines for using layers 1 to 6 of the LonTalk® protocol and the requirements for compatibility at Layer 1.
- *LONMARK Application Layer Interoperability Guidelines*. Provides guidelines for the LonTalk application layer, including the handling of functional blocks, configuration information, product documentation, SNVTs, and SCPTs.
- *The Echelon LONWORKS Products Catalog*, which contains a data sheet for all LONWORKS products, including Echelon's family of SMX transceivers.
- *The ShortStackUser's Guide*. Provides information on designing devices using the ShortStack Micro Server.

- *LonBuilder Microprocessor Interface Program (MIP) User's Guide*. Provides information for developing network interface applications with a generic LONWORKS network interface for use by others, or for developing a LONWORKS network interface for the user's own application.
- *LONWORKS FTT-10A Free Topology Transceiver User's Guide*. Describes the functions and operations of the FTT-10A free topology transceiver.
- *LONWORKS PLT-20 C-Band Power Line Transceiver Module User's Guide*. Describes the function and operation of the PLT-20 C-band power line transceiver module.
- *LPT-10 Link Power Transceiver User's Guide*. Describes the functions and operations of the LPT-10 transceiver.

2

Getting Started with the LTM-10A Platform

This chapter describes how to get started with the LTM-10A module by setting up the LTM-10A platform. This chapter also applies to LTM-10 Motherboard users.

Overview

The LTM-10A platform enables you to interface an LTM-10A Module to an SMX transceiver and a LONWORKS network without having to do any hardware development other than adding your application I/O.

To begin using the LTM-10A platform follow these steps:

1 Verify that your LTM-10A platform is complete. The platform requires the following components:

- LTM-10 motherboard with LTM-10A Module.
- Twisted pair cable for connecting the device to a twisted pair network (twisted pair version only).
- Wall-mount power supply (or your own +5VDC regulated power supply for use with the PLM-20 transceivers).
- Power supply cable for external regulated +5VDC supply.
- *LTM-10A User's Guide* (this manual).

Skip to step 6 if you purchased a NodeBuilder Development Tool or an assembled LTM-10A platform.

2 Verify that the LTM-10A module is installed in connectors J1 and J2 on the motherboard. To install the LTM-10A module, align the pins of the module with the sockets at positions J1 and J2 on the motherboard and press the module firmly into place. Secure the module to the metal standoffs with mounting screws.

3 Verify that an SMX transceiver is installed in the P1 connector on the motherboard. If not, install one using the following steps. First, remove the standoff and spacer at the front metal bracket, but save the mounting screw. Next, position the transceiver component side down over the motherboard so that the 20-pin connectors are aligned and the SMX transceiver's metal bracket is at the outside edge of the motherboard, on the same side as the J3 power jack. Press down firmly to set the connectors and the board down onto the motherboard's metal spacer. Finally, using the mounting screw, secure the transceiver onto the metal standoff. The following SMX transceivers are available from Echelon:

- Model 77010 TPM/XF-78 Twisted Pair Modular Transceiver
- Model 77030 TPM/XF-1250 Twisted Pair Modular Transceiver
- Model 77040 FTM-10 Free Topology Modular Transceiver
- Model 77160 PLM-22 C-Band Power Line Modular Transceiver

4 Set any option jumpers on the SMX transceiver by referring to the *LONWORKS SMX Transceivers* data sheet.

5 You also can use an SMX transceiver from a third party, or you can develop your own. See *Using a Non-Standard Transceiver* in Chapter 3 for information on how to configure the LTM-10A module for a non-standard transceiver. Transceivers for other media may be available from other suppliers. Consult the third party product listing at www.echelon.com/products for more information on third-party transceivers.

6 Attach the SMX-compatible transceiver to a LONWORKS network. The PLM-20 transceiver requires an external power line coupler for connection to the power mains. See the *LONWORKS Power Line Couplers* data sheet and the transceiver manuals for details.

7 Attach any I/O devices to the platform using the I/O connector at J5.

8 Apply power to the motherboard by attaching the wall-mount power supply output to connector J3. See *Connecting Power* in this chapter. If you are using a PLM transceiver, you must provide regulated +5VDC power on connector J4.

9 Develop and load an application on the LTM-10A Module. See *Programming the LTM-10A* in Chapter 4.

Attaching to a LONWORKS Network

The LTM-10A platform uses an SMX transceiver at P1 to connect to a LONWORKS network. Table 2.1 gives the pin out of the motherboard's P1 connector.

Table 2.1 P1 20 Pin SMX Transceiver Header

Name	***Function***	***Pin Number***
~PKT SEND	Flashes SMX LED on transmitted packets; output	18
CLK	Neuron Chip CLK2 output	17
CP0	Neuron Chip communication port 0	10
CP1	Neuron Chip communication port 1	8
CP2	Neuron Chip communication port 2	6
CP3	Neuron Chip communication port 3	12
CP4	Neuron Chip communication port 4	4
~RESET	Neuron Chip reset	16
XID0	Transceiver ID 0 input (LSB)	3
XID1	Transceiver ID 1 input	5
XID2	Transceiver ID 2 input	7
XID3	Transceiver ID 3 input	9
XID4	Transceiver ID 4 input (MSB)	11
V_{CC}	+5VDC output	1,19
GND	Ground	2,20
NC	No connect	13, 14, 15

Attaching I/O Devices

I/O devices are connected to the LTM-10 motherboard through connector J5. You may choose to use an Echelon Gizmo 4 I/O Board for early testing, or you can connect devices of your own design. The pinout of I/O connector J5 is given in table 2.2

Table 2.2 J5 20 Pin I/O Connector

Name	***Function***	***Pin Number***
IO0	Neuron Chip I/O Pin 0	1
IO1	Neuron Chip I/O Pin 1	2
IO2	Neuron Chip I/O Pin 2	3
IO3	Neuron Chip I/O Pin 3	4
IO4	Neuron Chip I/O Pin 4	5
IO5	Neuron Chip I/O Pin 5	6
IO6	Neuron Chip I/O Pin 6	7
IO7	Neuron Chip I/O Pin 7	8
IO8	Neuron Chip I/O Pin 8	9
IO9	Neuron Chip I/O Pin 9	10
IO10	Neuron Chip I/O Pin 10	11
~IRQ	LTM-10A Interrupt request to host	13
~SERVICE	Neuron Chip Service Pin	15
~RESET	Neuron Chip Reset Pin	16
V_{CC}	+5VDC output	19
GND	Ground	20
N/C	No Connect	12, 14, 17, 18

Connecting Power

The LTM-10 motherboard requires power as described below:

- *Primary Power*. For most configurations, primary power is supplied via the DC power jack at J3. This jack accepts unregulated +9 to 12VDC input, which the motherboard regulates to +5VDC. Connect the wall-mount power supply provided with the LTM-10A platform to this jack. This input can be used with any SMX transceiver that requires less than 100mA. The output of the LTM-10 power supply is a nominal 9-12VDC at 500mA. Table 2.3 lists the specifications of the LTM-10 power supplies.

Table 2.3 LTM-10A Platform Power Supplies

Country or Region	*Nominal Input Voltage*	*Input Range Nominal ±10%*	*Frequency*	*Input Connector*	*Echelon Model #*
North America	120 VAC	108-132 VAC	60 Hz	2-prong, NEMA 1-15P	78010
Japan	100 VAC	90 - 110 VAC	50/60 Hz	2-prong, NEMA 1-15P	78040
U.K.	240 VAC	216 - 264 VAC	50 Hz	3-prong, U.K. Plug	78030
Continental Europe	220 VAC	198 - 242 VAC	50 Hz	2-prong, Euro Plug	78020

- *Alternate Primary Power*. For SMX transceivers that require more than 100mA, such as power line transceivers, regulated +5VDC ±5% power must be supplied to the motherboard. In this case, only the DC power connector at J4 is used. Connect a regulated +5VDC ±5% power supply to J4, and do not use the wall-mount power supply included with the LTM-10A platform. Make sure the output current capability of your power supply is enough to satisfy the current needs of the SMX transceiver used. The J4 connector is compatible with IBM PC compatible disk drive power connectors so that a readily available PC power supply may be used.

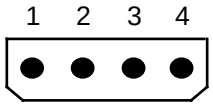


Figure 2.1 J4 Connector Front Panel View

Table 2.4 J4 Connector Pin Out

Name	*Function*	*Pin #*	*Color*
N/C	No connect	1	Yellow
GND	Ground	2	Black
GND	Ground	3	Black
V_{CC}	+5VDC input	4	Red

Using the LTM-10A Platform

The LTM-10A platform includes switches and indicators that are used as described in table 2.5. The LTM-10A module signals are described in Chapter 3.

Table 2.5 Motherboard Switches and Indicators

Name	*Label*	*Description*	*Usage*
Power LED	DS1	Green LED	Illuminated when power is on.
Service Button	S1	Pushbutton	Push to assert the ~SERVICE pin on the LTM-10A module. When pressed, the LTM-10A firmware will send a service pin message to the network. This pushbutton is also used in the application clearing procedure described in Chapter 4.
Service LED	DS2	Yellow LED	Displays the state of the LTM-10 ~SERVICE pin (active low).
Reset Switch	S2	Pushbutton	Push to assert the ~RESET pin on the LTM-10A module. When pressed, this switch resets the LTM-10A. This pushbutton is also used in the application clearing procedure described in Chapter 4.
Reset LED	DS3	Red LED	Displays the state of the LTM-10A ~RESET pin. A pulse stretcher ensures that brief reset pulses will be visible.
IO4 Switch	S3	Pushbutton	Push to ground the IO4 pin of the LTM-10A Module.
IO0 LED	DS4	Green LED	Buffered output displays the state of the LTM-10A IO0 line (active low).

LTM-10 Motherboard Schematic

The following schematics detail the LTM-10 motherboard.

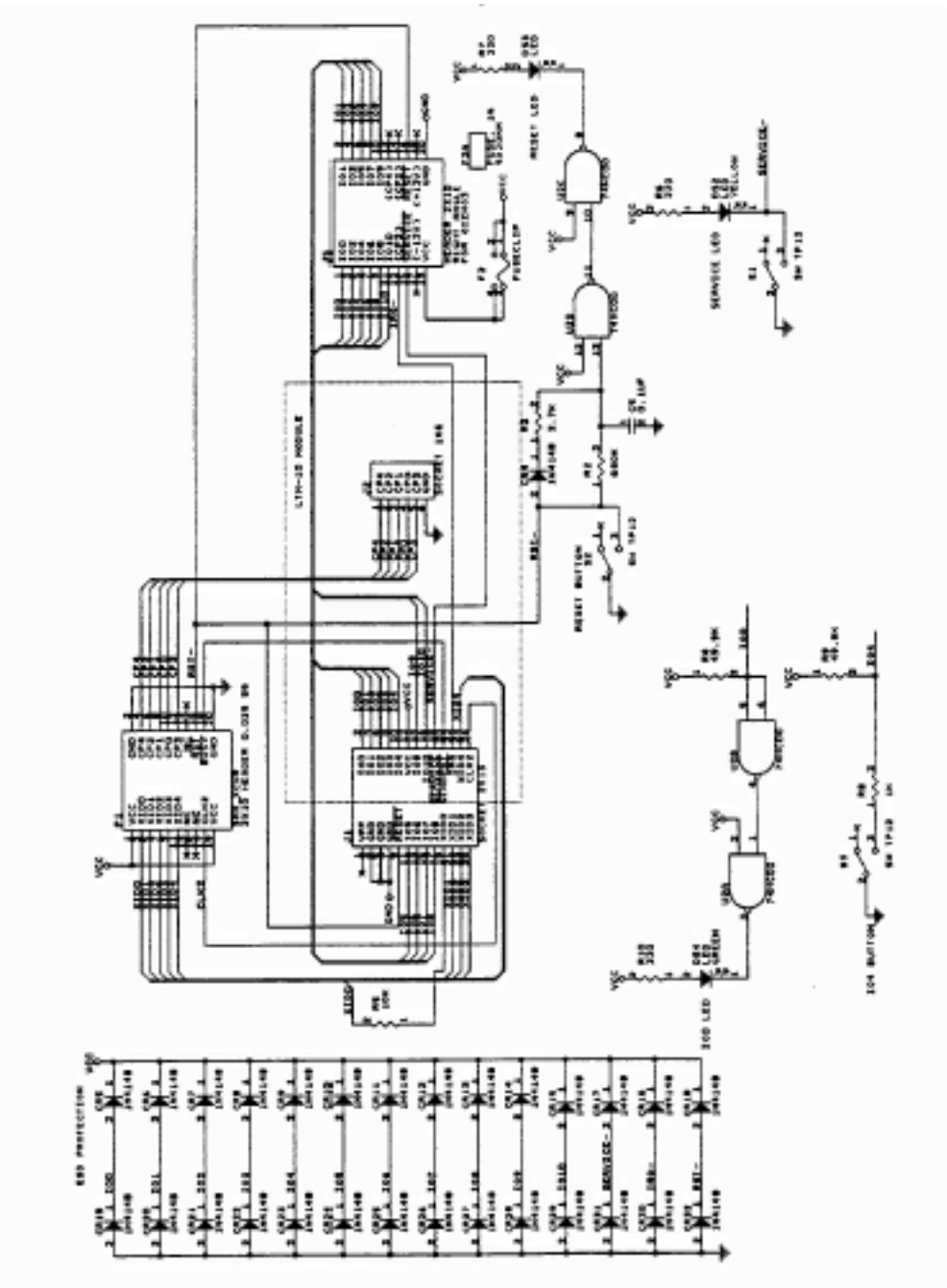


Figure 2.2 LTM-10 Motherboard Schematic (Part 1)

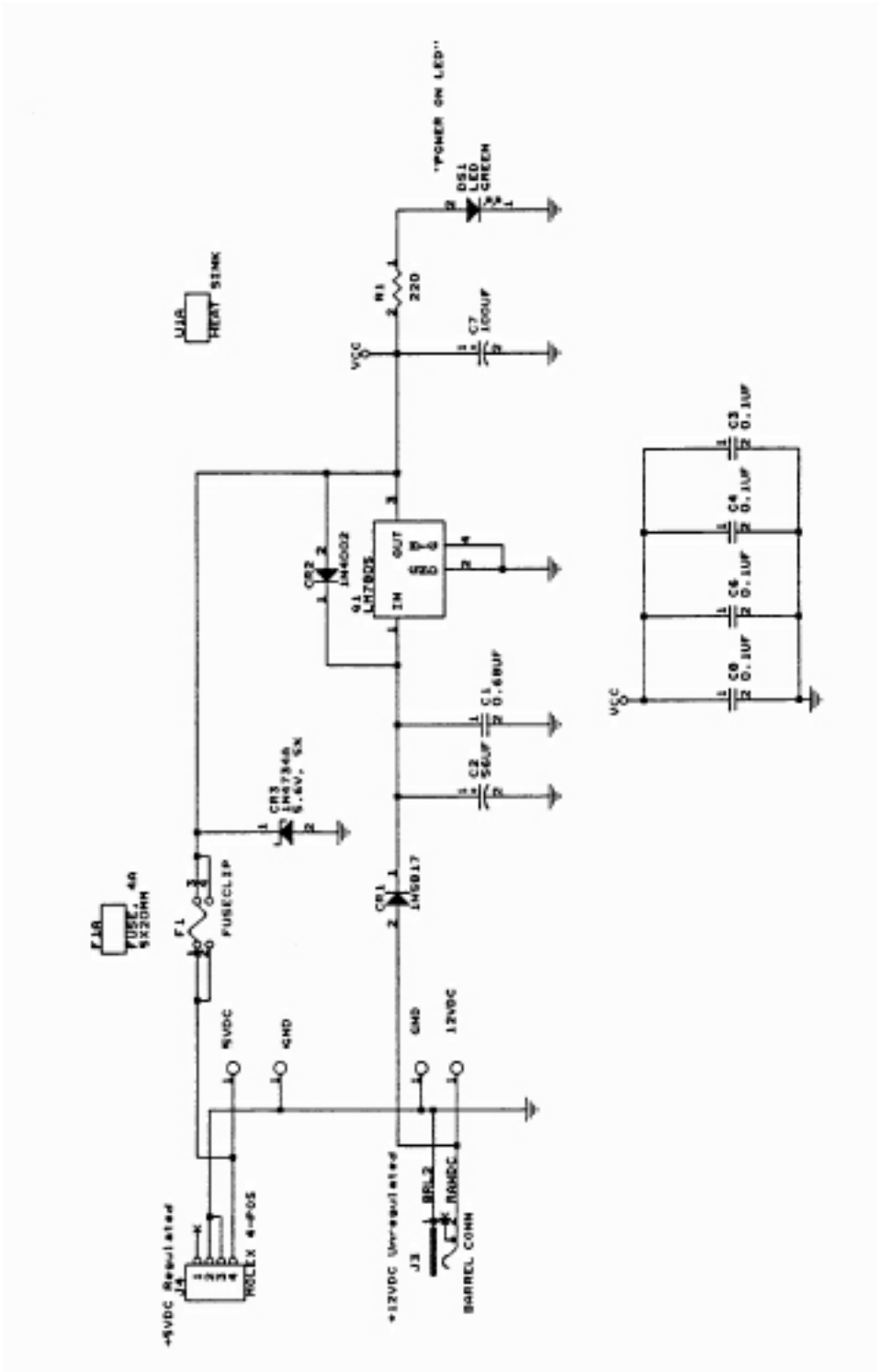


Figure 2.2 LTM-10 Motherboard Schematic (Part 2)

3

Designing in the LTM-10A Flash Control Module

This chapter describes the information necessary to design the LTM-10A module into your device. The LTM-10A Flash Control Module interfaces to the device application electronics and to the network through two connectors, P1 and P2, respectively.

Designing the Mechanical Interface

The LTM-10A flash control module footprint and connectors are shown in figure 3.2. The most common LTM-10A module mounting scenario uses socket strips on the application electronics board which connect with P1 and P2 as shown in figure 3.1. Vendor information for socket strips that mate with the 0.025" (0.64mm) square header posts of P1 and P2 is shown in table 3.1.

If necessary, taller socket strips may be used to gain more clearance between the LTM-10A module and the application board. Decisions about component placement on the application electronics board must also consider electromagnetic interference (EMI) and electrostatic discharge (ESD) issues discussed later in this document. Figure 3.2 shows the maximum height of parts on both sides of the LTM-10A module.

Three plated mounting holes that accept No. 6 (3.5mm) mounting screws are electrically connected to the LTM-10A module ground plane. When the 0.025" (0.64mm) square posts of P1 and P2 are inserted into the sockets they provide enough holding strength (3 oz (85g)/pin) to secure the LTM-10A module against shock and vibration to the operating limits of the components on the module. However, at least one metal standoff and fastening screw located at the mounting hole near the P2 connector is recommended to meet EMI limits and for ESD protection.

Figure 3.2 shows the recommended PCB pad layout for the application electronics board to interconnect an LTM-10A module with an application board that has socket strips mounted on the component side.

Table 3.1 Socket Strips Suitable for Use with the LTM-10A Module Header Pins

Manufacturer	***P1: 26-pin (2 X 13)***	***P2: 6-pin (1 X 6)***
Samtec	SSW-113-01-T-D	SSW-106-01-T-S
Augat		A010-006-YB-001
Methode		9000-106-303

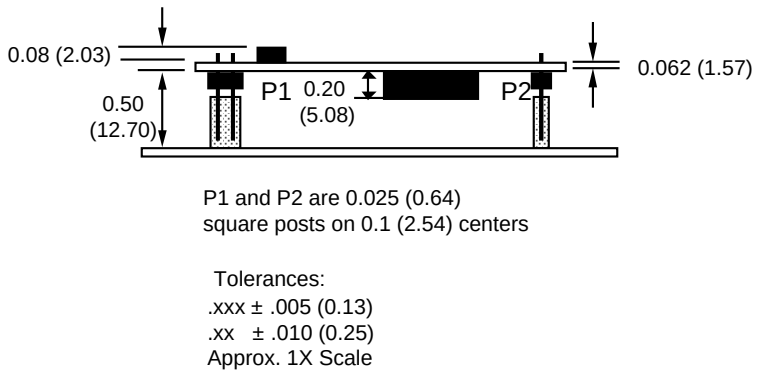
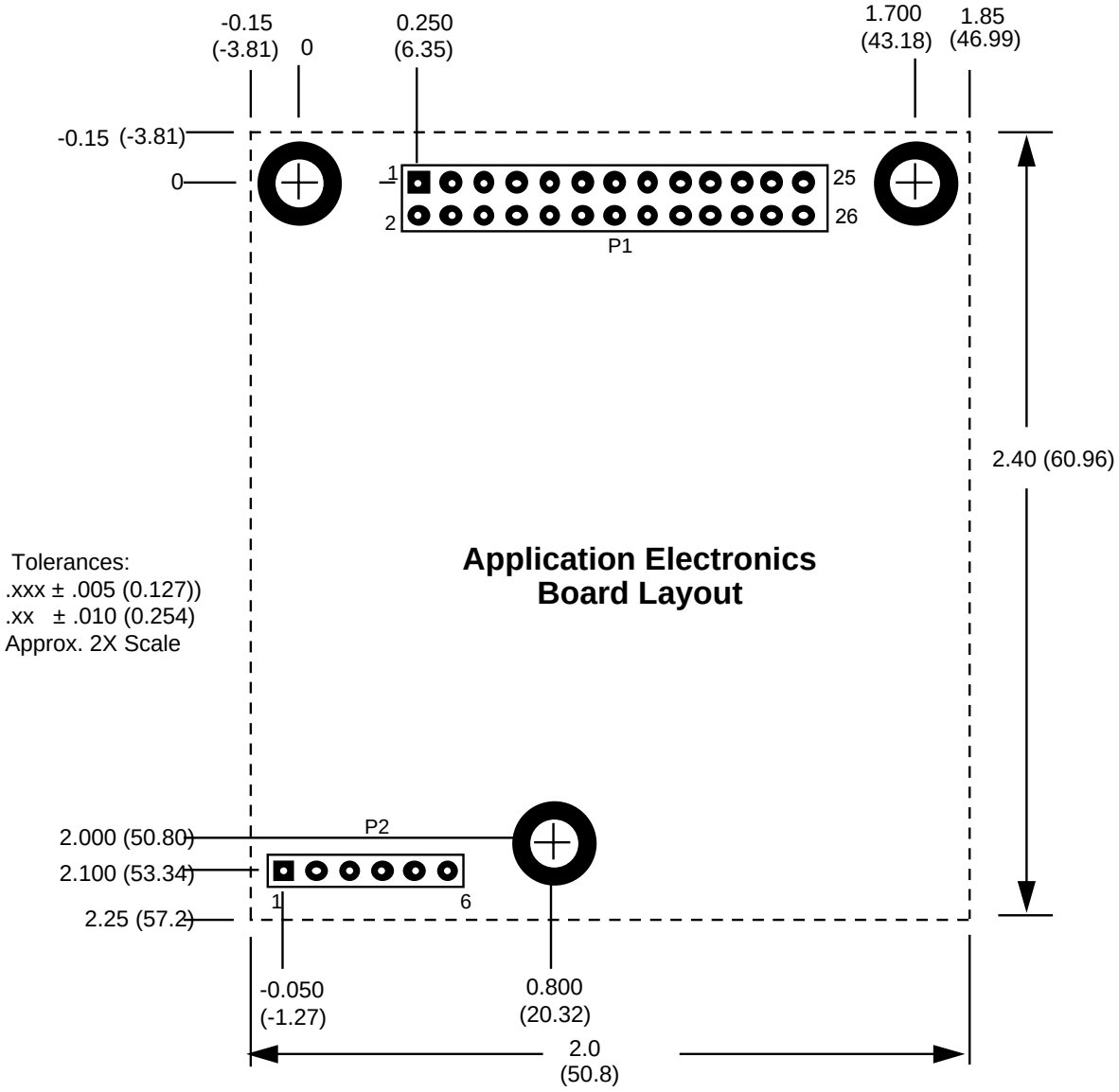


Figure 3.1 Recommended Spacing between the LTM-10A Module and Application Electronics Board



Reference	Pad O.D.	Finished Plated Hole Dia. ±0.003 (0.08)
Mounting	0.285 (7.24)	0.152 (3.86)
P1,P2	0.060 (1.52)	0.039 (0.99)

Figure 3.2 Required Pad Layout for Application Electronics Board

Designing the Electrical Interface

Table 3.2 summarizes the pins on the LTM-10A module. The following paragraphs provide a detailed description of each pin. All inputs require TTL-level inputs except as noted. Figure 3.2 identifies the pins on the motherboard.

Table 3.2 LTM-10A Module Pinouts

Name	***Description***	***Pin #***
~PKT SEND	LTM-10A activity output (8mA sink, 20 µA source)	P1-20
CLK OUT	Neuron Chip CLK2 output (CMOS level, drives 1 CMOS load))	P1-26
CP[4..0]	Network communication port	P2-1,5,2,3,4
IO[10..0]	Neuron Chip I/O Pins	P1-16,14,17,15,13, 11,10,8,6,4,2
~IRQ	Interrupt request output (CMOS level, 4mA sink)	P1-22
~RESET	Reset input and output	P1-9
~SERVICE	Service invocation input and service status output	P1-18
XID[4..0]	Transceiver ID inputs	P1-24,25,23,21,19
V_{CC}	+5VDC ±5% input	P1-12
GND	Digital ground	P1-3,5,7 P2-6
N/C	No connect; must be floating	P1-1

~PKT SEND

The ~PKT SEND output signal is asserted low when the LTM-10A module is sending a packet to the network. The ~PKT SEND output signal is asserted for approximately 40ms when the application processor of the Neuron Chip on the LTM-10A module queues a message for sending. This output can be used to drive an activity LED. It can sink 4mA with $V_{OL} \leq 0.45V$ or 20mA with V_{OL}~IV. It can source 20µA with $V_{OH} \geq 2.4V$.

CLK OUT

The CLK OUT output signal is driven by the CLK2 pin of the LTM-10A module Neuron Chip at the same frequency as the Neuron Chip CLK IN input. It is a CMOS driver that can drive 5 LS-TTL loads and can be used to interface to the FTT-10 Free Topology Transceiver and the LPT-10 Link Power Transceiver.

CP[4..0]

The CP[4..0] signals are connected to the CP[4..0] communications port pins of the Neuron Chip on the LTM-10A module. The function of these pins is described in the *Neuron Chip Data Book*.

IO[10..0]

The IO[10..0] signals are connected to the IO[10..0] pins of the Neuron Chip on the LTM-10A module. The Neuron Chip uses these pins to connect to application-specific I/O hardware. The specific functions of these pins is described in the *Neuron Chip Data Book*.

~IRQ

The IRQ signal output signals an interrupt request from the LTM-10A module to the host processor when executing the MIP/P50 firmware. It pulses high or low to signal an interrupt request. The polarity is under software control. It is also available for use by an application. The address of this memory mapped register is the least significant bit (LSB) of location 0xE000, and the state of the signal reflects the value written to this location, either a '0' or a '1'. See Chapter 4 for a Neuron C example using this output.

~RESET

The ~RESET signal resets the LTM-10A module and is asserted low by the LTM-10 low voltage protection circuit. An external low voltage protection circuit is not required. This signal may be directly connected to a reset push button without debouncing. Figure 3.3 shows the reset circuitry on board the LTM-10A module.

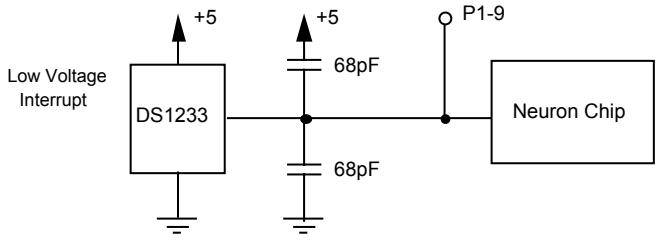


Figure 3.3 LTM-10A Module Reset Circuit

If this signal is driven by an external circuit, it must be driven by an open-collector or open-drain driver since the signal is both an input and an output.

The Reset pin is driven low by the Neuron Chip whenever the Neuron Chip is reset internally. When you load an application with the LonBuilder, NodeBuilder, or LonMaker™ tools, the Reset pin can flash periodically, indicating resets as part of the load process. When the Neuron Chip's watchdog timer expires, the Reset pin is also asserted low by the Neuron Chip.

When used as a MIP module, the Reset output of the LTM-10 must be used to alert the attached host processor that the host interface must be resynchronized.

~SERVICE

The ~SERVICE signal is connected to the ~SERVICE pin of the LTM-10A module's Neuron Chip. The function of the ~SERVICE pin is described in the *Neuron Chip Data Book*. The internal pullup resistor for the service pin is enabled by the LTM-10 firmware. A service LED driven by the ~SERVICE signal will reflect the LTM-10 firmware status: *blinking* means that the LTM-10A module is unconfigured, *off* means that it is configured, and *on* means that the node is applicationless.

Typical applications do not require debounce conditioning of momentary push buttons attached to the ~SERVICE pin. The software response time associated with this input is long enough to effectively provide a software debounce for switches with a contact bounce time as long as 20ms.

The condition of the service LED may be observed for clues about the actual state of the node. The behavior of the service LED, specifically the duration of ON and OFF states, varies depending on the operating state of the node.

Figure 3.4 illustrates the different service LED behavior alternatives. These are the most common behaviors, others are possible since the state of the service LED is under firmware control and can be affected by both hardware and software anomalies. The state of the service LED can also be affected by the application program using the activate_service_led built-in variable.

Table 3.3 describes each of the behaviors shown in figure 3.4 under different contexts. Again, this list is not exhaustive and therefore does not provide explanations for every possible service LED behavior.

Behavior 7 represents that of a fully configured node during normal operation.

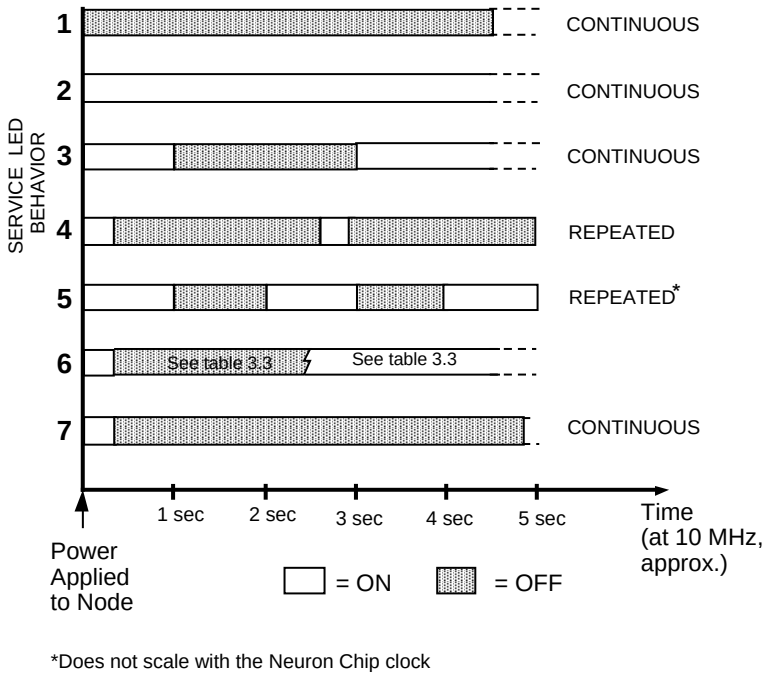


Figure 3.3 Possible Service LED Behaviors Showing Different Duty Cycles

Table 3.3 Explanation of the Service LED Behaviors Shown in Figure 3.3

BEHAVIOR	CONTEXT	LIKELY EXPLANATION
1	Power-up	Bad device hardware
2	Power-up	Bad device hardware
3	Power-up/Reset	Device is applicationless May be caused by the Neuron Chip firmware when a mismatch occurs on application checksums This behavior is normal if the application was exported to come up applicationless
4	Anytime	Watchdog timer resets occurring Possible corrupt EEPROM Make the Neuron Chip applicationless by holding down the service button and then pressing and releasing the reset button. Hold the service button down until the reset LED flashes a second time. See Chapter 4.
5	Anytime	Device is unconfigured but has an application. Proceed with loading the device.
6	Using EEBLANK	The OFF duration is approximately 10 seconds (10MHz Neuron Chip). This duration scales proportionally to the system clock. After this OFF time the service LED should turn ON and stay ON, indicating the completion of the blanking process
6	First power up with a new flash on a Neuron 3150 Chip-based custom device. Applicationless firmware state exported	The OFF duration is approximately 1 second. Service LED should then turn ON and stay on indicating an applicationless state
6	First power up with a new flash. Unconfigured firmware state exported	The OFF duration is 1-15 seconds depending on the application size and system clock. Service LED should then begin flashing as in behavior 5 shown in figure 3.3, indicating an unconfigured state
6	First power up. Configured firmware state exported	The OFF duration is indefinite (1-15 seconds to load internal EEPROM; stays OFF indicating configured state.)
7	Anytime	Device is configured and running normally

XID[4..0]

The LTM-10A module comes preconfigured with many common LONWORKS transceiver parameters. The XID[4..0] input signals specify a transceiver identification (ID) to select the appropriate transceiver type.

The transceiver ID inputs simplify LTM-10 configuration by automatically configuring the LTM-10A module for most transceivers. A special transceiver ID is reserved for programming any custom transceiver type. This value causes the communication port pins to be configured as all inputs so that no line will be driven by both the transceiver and the LTM-10A module before the LTM-10A can be properly configured. See *Using a Non-Standard Transceiver* later in this chapter.

The LTM-10A module reads the transceiver ID inputs on power up and reset. If it is being powered-up for the first time, or if the transceiver ID is different from the last time it was powered-up, the parameters specified in table 3.4 are loaded. If it is not being powered-up for the first time, and the transceiver ID is not 30, the LTM-10A module compares the network bit rate and input clock for the specified transceiver to the current transceiver parameters. If these parameters don't match, then all transceiver parameters are reinitialized. These inputs must be tied high or low. They cannot be left floating.

Table 3.4 LTM-10 Transceiver Parameters

ID	*XID(4..0)*	*Name*	*Media*	*Network Bit Rate*	*Input Clock*	*# of Priority Slots*
01	00001	TP/XF-78	Transformer-isolated twisted pair	78kbps	10MHz	4
03	00011	TP/XF-1250	Transformer-isolated twisted pair	1.25Mbps	10MHz	16
04	00100	TP/FT-10	Free topology with optional link power	78kbps	10MHz	4
05	00101	TP/RS485-39	RS-485 twisted pair	39kbps	10MHz	4
10	01010	TP/RS485-625	RS-485 twisted pair	62kbps	10MHz	4
11	01011	TP/RS485-1250	RS-485 twisted pair	1.25Mbps	10MHz	16
12	01100	TP/RS485-78	RS-485 twisted pair	78kbps	10MHz	4
15	01111	PL-20A	A-band power line	2613bps	10MHz	8
16	10000	PL-20C	C-band power line[1]	5kbps	10MHz	6
17	10001	PL-20N	C-band power line[1]	5kbps	10MHz	8
27	11011	DC-78	Direct connect	78kbps	10MHz	0

[1] PL-20C enables the CENELEC compliant access protocol; PL-20N disables it

28	11100	DC-625	Direct connect	62kbps	10MHz	0
29	11101	DC-1250	Direct connect	1.25Mbps	10MHz	0
30	11110	Custom	Custom[1]	N/A	N/A	0

Using Pre-Defined Transceivers

The LTM-10A module includes pre-defined transceiver parameters for the transceivers listed in table 3.4. When using any of these transceivers, the transceiver parameters are automatically programmed as described under the description of the XID[4..0] signals in this chapter.

The following sections describe the hardware interface for standard LONWORKS transceivers available from Echelon for free topology, twisted pair, and power line communications. The user's guide for each transceiver contains documentation on the interface requirements. The following sections provide additional information on using these transceivers with the LTM-10A module.

> Note: The user's guides for the various transceivers are the source material for all reference information. The following schematics are **samples** and are provided for example purposes only.

FTT-10A Free Topology Transceiver

The FTT-10A Free Topology Transceiver supports polarity-insensitive communications over twisted pair cable with any topology, including bus, star, loop, and hybrid wiring. It is compatible with Echelon's LPT-10 Link Power Transceiver, and these transceivers can communicate with each other on a single twisted pair cable. Figure 3.5 shows the interface between the FTT-10A and LTM-10A modules. The transceiver ID must be set to 4 as shown in the schematic. See the *LONWORKS FTT-10A Free Topology Transceiver User's Guide* for additional information.

[1] Use type 30 for any transceiver type. The communications port is initially defined as all inputs. This option is not supported by the NodeBuilder software.

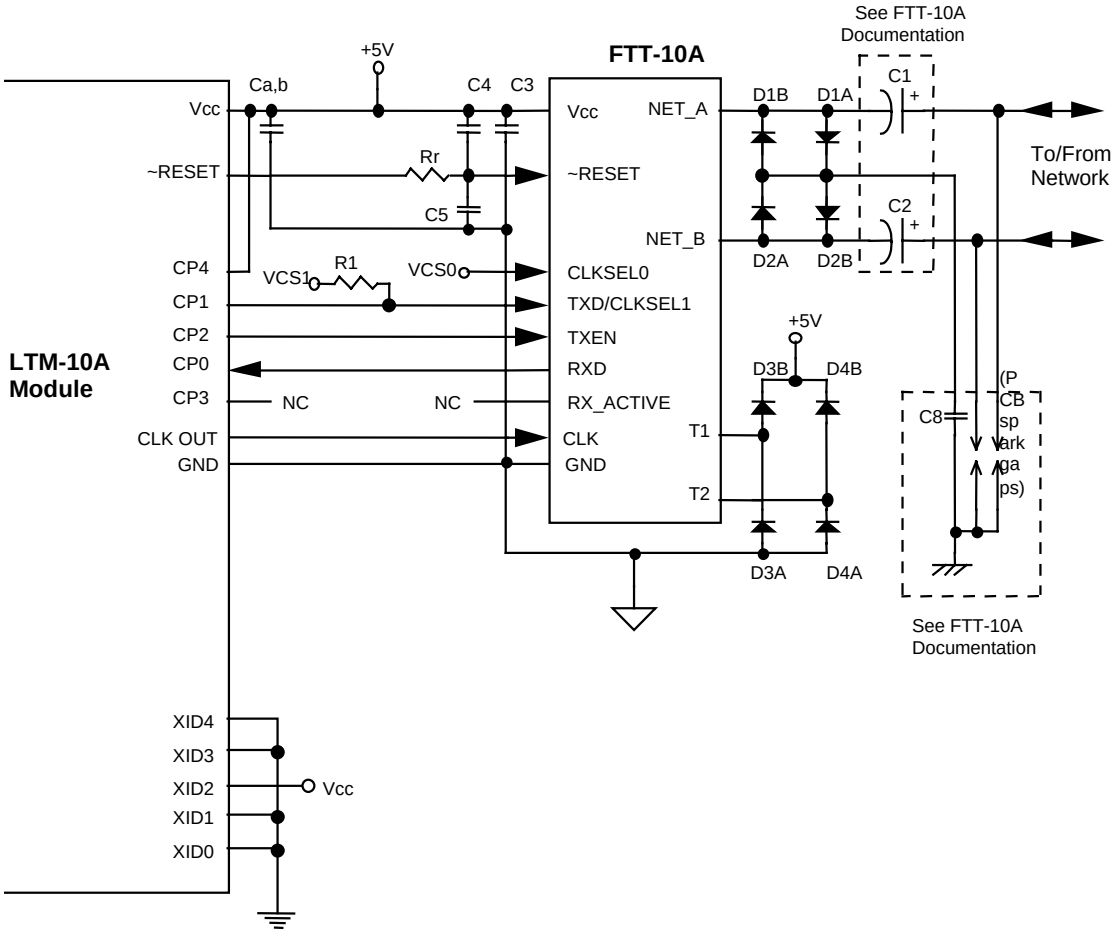


Figure 3.5 Sample FTT-10A Transceiver Interface

Power Line Transceiver

The PLT-20 Power Line Transceiver supports communications over AC or DC power mains. It may be connected to the LTM-10A module and a coupling circuit as shown in figure 3.6. The transceiver ID input must be set as shown. See the *LONWORKS PLT-20 C-Band Power Line Transceiver Module User's Guide* for additional information, including a description of the coupling circuits.

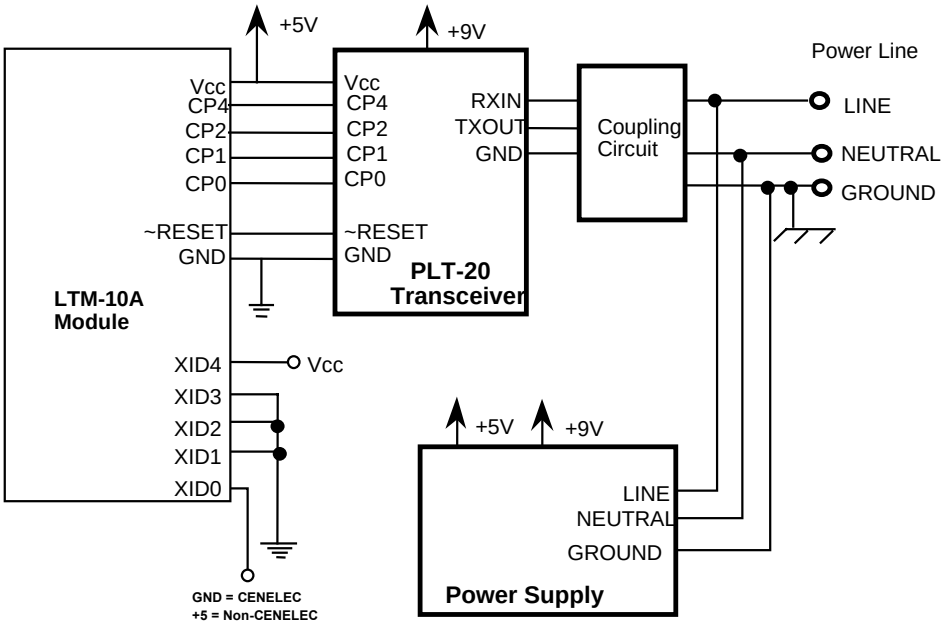


Figure 3.6 Sample PLT-20 Transceiver Interface

TPT/XF-78 and TPT/XF-1250 Twisted Pair Transceivers

The TPT/XF-78 and TPT/XF-1250 transceivers support polarity-insensitive communication over twisted pair cable with a bus topology. The connection between the LTM-10A module and the TPT/XF-78 and TPT/XF-1250 Twisted Pair Transceivers is shown in figure 3.7.

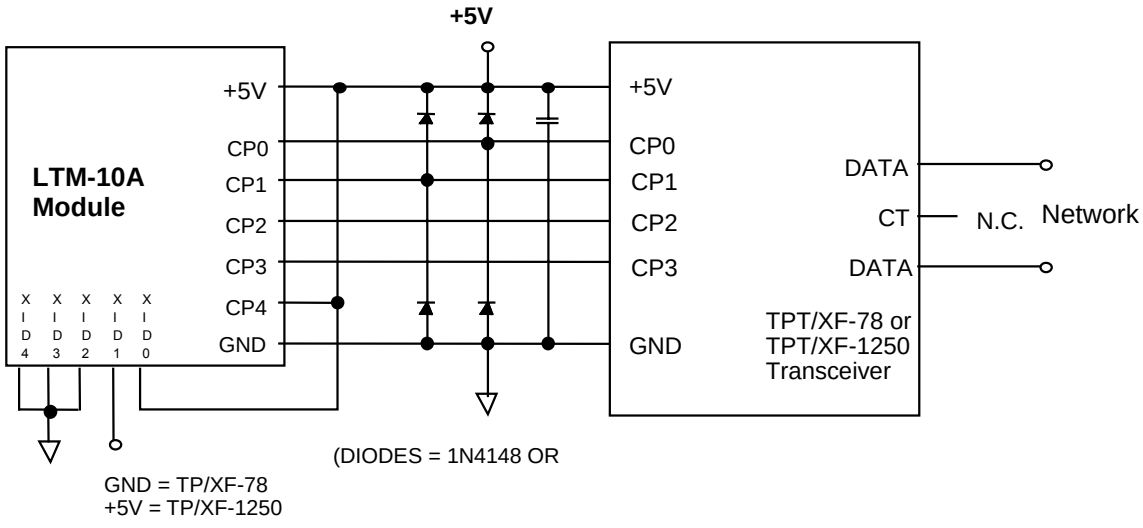


Figure 3.7 Connection between LTM-10A Module and TPT/XF-78 or TPT/XF-1250 Twisted Pair Transceivers

Using Custom Transceivers

The LTM-10A module can be used with transceivers not listed in table 3.4 as long as the communication parameters are programmed to match the custom transceiver. You must use the custom transceiver type (ID 30) for the LTM-10A module and load the appropriate communications parameter into the module via the MIP interface.

Optionally, you may load the new communication parameters over the network using a LonBuilder system and the following steps:

1. Place a standard LonBuilder transceiver in the network manager slot.
2. Install the network manager using the appropriate standard transceiver for its channel description.
3. Define a logical phantom router in the LonBuilder. Assign the same transceiver type as the one used for the network manager node to one side of the router. The other side of the router should be assigned the channel that represents your custom transceiver. There is no need for the actual router hardware to be present for this step.
4. Connect your LTM-10A to an SMX transceiver that matches the transceiver in the LonBuilder network manager. The SMX transceiver will set the appropriate transceiver ID for the LTM-10A.
5. Connect the LTM-10A Platform to the network manager and install it. Respond **`YES`** when asked to have the communication parameters loaded.
6. Disconnect the module from the network, remove power from it, and replace the SMX transceiver with your custom transceiver.
7. Choose the custom transceiver type (ID 30) for your LTM-10A.
8. Your LTM-10A is now programmed with your custom communication parameter.

Compatibility with Other Control Modules

The LTM-10A module is compatible with the Echelon control modules. Pins 1 through 18 of the P1 connector are identical to those of the same connector on the TP/XF-78, TP/XF-78F, TP/XF-1250, TP/FT-10 and the TP/FT-10F modules. Therefore, you can design a motherboard that will accommodate all these modules. Special attention must be given to the physical size of the LTM-10A module as it is wider than the other control modules. Refer to the *LONWORKS Twisted Pair Control Module User's Guide* for mechanical and electrical specifications of these control modules.

Providing Power

The LTM-10A Flash Control Module requires a +5VDC power source with sufficient current to power the LTM-10A module in all modes of operation.

The supply current requirements for the LTM-10A module are outlined in table 3.5. The LTM-10A module requires a +5VDC ±5% power supply.

Table 3.5 LTM-10A Module +5 Volt Current Requirements

	Typical	Max
Current consumption @ 10MHz	100mA	160mA

Notes:

1. Assumes internal I/O pullups are disabled and I/O lines are not connected to a load.
2. Assumes ~SERVICE pullup is enabled.
3. Includes CMOS flash memory running typical application with the Neuron Chip firmware.
4. Actual current consumption of the LTM-10A Flash Control Module will depend on the load characteristics of the transceiver with which it is used.

Power Supply Decoupling and Filtering

The design for the LTM-10A module power supply must consider filtering and decoupling requirements of the LTM-10A module. The power supply filter must prevent noise generated by the LTM-10A module and I/O circuits from conducting onto external wires, and in the case of DC-DC switching power supplies, must prevent noise generated by the supply from interfering with module operation. Switching power supply designs must also consider the effects of radiated EMI.

The LTM-10A module includes 2.2µF and 0.1µF power supply bypass capacitors on the +5V supply line. In general, a high frequency decoupling capacitor valued at 0.1µF or 0.01µF placed near pin 12 of P1 on the motherboard is necessary to reduce EMI.

The LTM-10A module requires a clean power supply to prevent RF noise from conducting on to the network through active drive circuits. Power supply noise near the network transmission frequency may degrade network performance.

Attention to the design of the application electronics circuit is also necessary. High-speed signals and inductive loads are common sources of noise which must be managed by separating the logic and I/O power supplies, or by using sufficient filtering and decoupling techniques.

Minimizing Electromagnetic Interference

The high-speed digital signals associated with microcontroller designs can generate unintentional Electromagnetic Interference (EMI). High-speed voltage changes generate RF currents that can cause radiation from a product if a length of wire or piece of metal can serve as an antenna.

Products that use the LTM-10A module will generally need to demonstrate compliance with EMI limits enforced by various regulatory agencies. In the USA, the FCC requires that unintentional radiators comply with Part 15 level "A" for industrial products, and level "B" for products that can be used in residential environments. Similar regulations are imposed in most countries throughout the world.

Echelon has designed the LTM-10A Flash Control Module with low enough RF noise levels for design into level "B" products. Echelon encourages level "B" compliance for all LONWORKS-compatible products.

Information on designing products for Electromagnetic Compatibility (EMC) is available in several forms including books, seminars, and consulting services. Echelon recommends the document *Electromagnetic Compatibility for Industrial-Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements*, IEC801-2,1991-04, draft.

Following are design tips for EMC:

- Most of the RF noise originates in the CPU portion of the LTM-10A module, and in any high-frequency or high-speed application circuitry in the node.
- Most of the Electromagnetic Interference (EMI) will be radiated by the network cable and the power cable.
- Filtering is generally necessary to keep RF noise from getting out on the power cable.
- The LTM-10A module must be well grounded within the node to ensure that its built-in EMI filtering works properly.
- Early EMI testing of prototypes at a certified outdoor range is an extremely important step in the design of level "B" products. This testing ensures that grounding and enclosure design questions are addressed early enough to avoid most last-minute changes (and their associated schedule delays).

The three standoff holes on the LTM-10A module are generally not needed for mechanical support, but the hole nearest connector P2 is important for EMI grounding of the LTM-10A module. Best results are achieved by a solid ground connection from the LTM-10A module to the application mother board and to a metalized enclosure using the P2 standoff.

Since the LTM-10A module routes the Neuron Chip's CP lines directly to connector P2 without filtering, your design may require filtering on the transceiver's network data communication lines to meet level "B" emission limits. In rare cases, such as designs including circuits with extremely fast edges, additional noise attenuation is

required. In such cases it may be necessary to use a common-mode choke, such as muRata's PLT1R53C connected in series with the data communication lines adjacent to the node's external network connector. This choke will provide an additional 10dB-to-15dB of EMI attenuation over the 30-to-500 MHz range. The choke adds a few pF of differential capacitance to the data communication lines, and therefore reduces network performance and may affect interoperability. In general, application designs should not require a common-mode choke.

Designing for Electrostatic Discharge Immunity

Electrostatic Discharge (ESD) is encountered frequently in industrial and commercial use of electronic systems (refer to *UL's LAN Cable Certification Program*, Document number 200-120 20M/11/91, by Underwriters Laboratories, Northbrook Illinois, (708) 272-8800). Reliable system designs must consider the effects of ESD and take steps to protect sensitive components. Static discharges occur frequently in low-humidity environments when operators touch electronic equipment. The static voltages generated by humans can easily exceed 10kV. Keyboards, connectors, and enclosures provide paths for static discharges to reach ESD sensitive components such as the Neuron Chip.

ESD hardening includes the following techniques:

- Provide adequate creepage and clearance distances to prevent ESD hits from reaching sensitive circuitry.
- Provide low impedance paths for ESD hits to ground.
- Use diode clamps or transient voltage suppression devices for accessible, sensitive circuits.

The best protection from ESD damage is circuit inaccessibility. If all circuit components are positioned away from package seams, the static discharges can be prevented from reaching ESD sensitive components. There are two measures of "distance" to consider for inaccessibility: creepage and clearance. Creepage is the shortest distance between two points along the contours of a surface. Clearance is the shortest distance between two points through the air. An ESD hit generally arcs farther along a surface than it will when passing straight through the air. For example, a 20kV discharge will arc about 0.4 inches (10mm) through dry air, but the same discharge can travel over 0.8 inches (20mm) along a clean surface. Dirty surfaces can allow arcing over even longer creepage distances.

When ESD hits to circuitry cannot be avoided through creepage, clearance and ground guarding techniques, i.e., at external connector pins, explicit clamping of the exposed lines is required to shunt the ESD current. Consult *Protection of Electronic Circuits from Overvoltages*, by Ronald B. Standler, for advice about ESD and transient protection for exposed circuit lines. In general, exposed lines

require diode clamps to the power supply rails or zener clamps to chassis ground in order to shunt the ESD current to ground while clamping the voltage low enough to prevent circuit damage. The Neuron Chip's I/O and control lines are connected directly to P1 without any ESD protection beyond that provided by the Neuron Chip itself. If these lines will be exposed to ESD in an application, protection must be added on the application electronics board. Figure 3.8 shows an example of the use of diode clamps to protect the LTM-10A module I/O lines in a keypad scanning application.

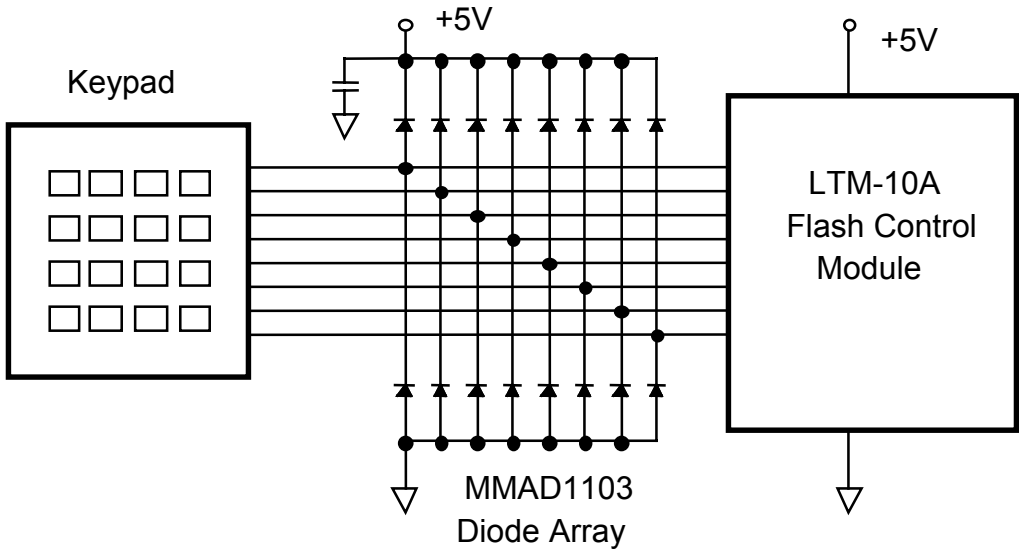


Figure 3.8 Example of Diode Clamping Protection for LTM-10A Module I/O Lines

4

Programming the LTM-10A Module

This chapter discusses the steps necessary for programming the LTM-10A module. Separate procedures are outlined for the LonBuilder and NodeBuilder tools.

LTM-10A Memory Maps

As described in Chapter 1, the LTM-10A module includes a 64Kbyte flash memory and a 32Kbyte RAM that may be allocated to the available 56Kbyte address space on the LTM-10A module (the upper 8Kbytes are reserved for I/O and on-chip Neuron memory on the LTM-10A module).

The LTM-10A firmware supports four memory maps. The LTM-10A firmware automatically selects the appropriate memory map when an image is downloaded to the LTM-10A module. All four memory maps always map the lower 16Kbytes of the flash memory to the lower 16Kbytes of the LTM-10A module. These 16Kbytes contain the Neuron firmware and the MIP/P50 image. The following table summarizes the memory allocation for the four memory maps:

Memory Map Name	***Flash Memory***	***RAM***
LTM-10A Flash	0 – 7FFF (32K)	8000 – DFFF (24K)
LTM-10A Flash 64K	0 – DFFF (56K)	None
LTM-10A MIP	0 – 3FFF (16K)	4000 – BFFF (32K)
LTM-10A RAM	0 – 3FFF (16K)	4000 – BFFF (32K)

The four memory maps support the following different types of applications:

- *LTM-10A Flash*. This memory map is used to run applications that require more RAM than the 2Kbytes of on-chip RAM on the LTM-10A Neuron Chip. The application is loaded in the 16Kbyte external flash, plus the available portion of the 2Kbyte EEPROM on the LTM-10A Neuron Chip. It can be used for debugging with the NodeBuilder 3 Development Tool, but if you will be doing extended debugging, you should use the LTM-10A RAM memory map instead. This memory map stores the application in non-volatile memory, so the application is preserved even if power to the LTM-10A module is lost or interrupted.

- *LTM-10A Flash 64K*. This memory map is similar to the LTM-10A Flash memory map, but supports a larger application (40Kbytes external flash memory instead of 16Kbytes external flash memory), and no external RAM. As with the LTM-10A Flash memory map, this memory map can be used for debugging with the NodeBuilder 3 Development Tool, but if you will be doing extended debugging, you should use the LTM-10A RAM memory map instead. This memory map stores the application in non-volatile memory, so the application is preserved even if power to the LTM-10A module is lost or interrupted.

- *LTM-10A MIP*. This memory map is used when the MIP/P50 image on the LTM-10A module is used to support an external host processor as described in Chapter 3.

- *LTM-10A RAM*. This memory map is used for application development using the NodeBuilder 3 Development Tool. The RAM memory map is ideal for

NodeBuilder development because the NodeBuilder debugger performs many writes to the application memory, and these frequent writes could ultimately cause a flash memory to fail. The RAM supports an unlimited number of writes, eliminating any limitations on debugging. The limitation of this memory map is that the application loaded into the LTM-10A module is lost if power to the module is lost or interrupted.

The LTM-10A RAM memory map should be used whenever you will be doing extensive debugging using the NodeBuilder debugger. This is because flash memory devices support a limited number of write cycles to each 128-byte sector, and the debugger performs frequent writes to the same sector when you are single-stepping through an application. See the Atmel databook for documentation on the write-cycle limitation of the AT29C512 flash memory device used on the LTM-10A module.

Using the LTM-10A Module with the LonBuilder Tool

You can use the LTM-10A module or LTM-10A Platform with the LonBuilder tool. To use either LTM-10A product with the LonBuilder tool, follow these steps:

1. Download the version 121 Ltm10sys.sym file from the Development Tools updates section in the Echelon Developer's Toolbox at www.echelon.com/toolbox.

2. Copy the Ltm10sys.sym file to a new Ver121 directory in the LonBuilder Images directory (c:\lb\images by default).

3. Copy the Gen.lib file from your LonBuilder Images\Ver6 directory to the new Images\Ver121 directory.

4. Create a hardware properties definition for the LTM-10A module specifying a Neuron 3150 Chip, 10MHz input clock rate, Ltm10sys firmware image, and 121 firmware version number.

5. Select a memory map as defined in LTM-10A Memory Maps earlier in this chapter. Define memory properties that match the entry in Table 4.1 for your selected memory map.

Table 4.1 LonBuilder Memory Settings

Memory Map Name	*ROM*	*EEPROM Or Flash*	*Memory Type*	*RAM*	*I/O*
LTM-10A Flash	None	Start: 0 Pages: 128	Flash 128-byte sector	Start: 8000 Pages: 64	Start: E000 Pages: 1
LTM-10A Flash 64K	None	Start: 0 Pages: 224	Flash 128-byte sector	None	Start: E000 Pages: 1
LTM-10A MIP	Start: 0 Pages: 64	None	Flash 128-byte sector	Start: 4000 Pages: 128	Start: E000 Pages: 1
LTM-10A RAM	Start: 0 Pages: 64	Start: 4000 Pages: 64*	EEPROM 0ms write time	Start: 8000* Pages: 64*	Start: E000 Pages: 1

* These numbers can be adjusted to change the mix of application vs. data RAM, as long as the non-volatile memory starts at 0x4000, the total number of pages is less than 128, and memory is not allocated past 0xBFFF.

6. Provide a logical and physical path from the LonBuilder network manager to the LTM-10A device. This will require a router if the LonBuilder network manager and the LTM-10A device do not use the same type of transceiver. The router may be a LonBuilder Router or a LonPoint Router with the appropriate transceivers on both sides to route between the two media. For example, if your LonBuilder network manager is using a backplane transceiver operating at 1.25MBps and your LTM-10A device is using an FTM-10 SMX transceiver, your router must have one of each of these two transceiver types. You must also configure and load this router using the LonBuilder software. Refer to the *LonBuilder User's Guide* for more information on installing and configuring LonBuilder routers. Refer to the *LonPoint Module Hardware and Installation Guide* for more information on installing and configuring LonPoint routers.

7. Install the LTM-10A device with the LonBuilder software. If your channel definition for the LTM-10A device uses a standard transceiver type, you do not need to update the communications parameters during installation. The LTM-10A module automatically configures its communications parameters based on input from its transceiver ID pins (the SMX modular transceivers automatically set the LTM-10A module transceiver ID pins when using an LTM-10 Motherboard).

8. Load the application over the network.

Using the LTM-10A Module with the NodeBuilder Tool

You can use the LTM-10A module or LTM-10A Platform with the NodeBuilder tool. Starting with the NodeBuilder 3 Development Tool, the NodeBuilder tool includes hardware templates that support the four LTM-10A memory maps described in *LTM-10A Memory Maps* earlier in this chapter. To use the LTM-10A module with the NodeBuilder tool, build an application as described in the *NodeBuilder User's Guide* using one of the four LTM-10A hardware templates. Do not use the LTM-10 templates; these are used with the original LTM-10 module that had a 16Kbyte flash memory instead of the 32Kbyte flash memory on the LTM-10A module.

You will typically use the **LTM-10A RAM** hardware template for your development target since it supports an unlimited number of write cycles to the application memory space, which is important while debugging your application. This template assigns the first 16Kbytes of the LTM-10A RAM as application memory, and the remaining 16Kbytes as RAM. You can change the mix of application memory and RAM. To do this, copy the **LTM-10A RAM** template to a user template, open the user template, and change the non-volatile and RAM settings on the Off-chip Memory tab. The non-volatile memory must start at 0x4000, the total memory allocated to non-volatile memory and RAM cannot exceed 32K, and memory cannot be allocated past 0xBFFF.

You will typically use the **LTM-10A Flash** or **LTM-10A Flash 64K** hardware template for your release target, depending on whether you need more flash memory or more RAM.

When you download your application to the LTM-10A module, the memory map on the LTM-10A module will automatically be initialized to match your selected hardware template.

LTM-10A Software Features

The LTM-10A firmware has several built-in features to simplify the development phase of a LONWORKS device.

Device Recovery

This feature, through a series of user-initiated steps, clears the application in the LTM-10A module and leaves the device in the applicationless state. This provides an easy way of returning the device to a known state in case of errors during development. The necessary steps are:

1 Activate the Service signal by depressing the Service switch and holding it depressed

2 Reset the LTM-10A module by depressing and releasing the Reset switch

3 Wait approximately ten seconds while still holding the Service switch depressed

4 Once the Reset LED flashes momentarily, release the Service switch

5 The device is now applicationless (Service LED is ON solid)

Activity LED

The ~PKT SEND signal (pin 20 of P1) is asserted low for approximately 40ms when a packet is sent from the network processor to the MAC processor on the LTM-10A device's Neuron Chip. This provides an indication of LTM-10-generated network activity for the LTM-10 device. For convenience, SMX-compatible transceivers have a front panel activity LED which can be driven by the ~PKT SEND signal from the LTM-10A module.

Interrupt Request Output

An additional memory mapped output signal is available on the LTM-10A module (pin 22 of P1) that can be used by the application program. This IRQ output, mapped to the LSB of address 0xE000, can also be used by the MIP/P50 on the LTM-10A module to interrupt the host. Refer to the *Microprocessor Interface Program User's Guide* for more information on the use of the uplink interrupt.

For a non-MIP application running on the LTM-10A module, the state of the IRQ pin can be controlled by the value written to the least significant bit of location 0xE000 (either a '0' or a '1'). The following Neuron C syntax can be used to set the state of the IRQ output signal:

```
unsigned int irq_out;               // the output value
*(unsigned short *)(0xE000) = irq_out;
```

5

Using the LTM-10A Module as a Network Interface

This chapter discusses the use of the LTM-10A module as a network interface. The necessary hardware and software components for interfacing the LTM-10A module to a host processor are discussed. In addition, a sample interface design is presented.

Building and Loading the MIP Application for the LTM-10A Module

During the load process, the LonBuilder or NodeBuilder software will load the MIP application over the network into the LTM-10A module. Aside from the configuration data, this consists of the small amount of code that is generated from the Neuron C source file. The reset task of this program calls the MIP function `mip_nb_interface()`, which is resident in the system image in the LTM-10A module's flash memory. The arguments to this function are the token throttle delay (in units of 350µs per count), and the address of a user-supplied function that the MIP calls to generate the uplink interrupt.

Once the MIP application is loaded, the LonBuilder or NodeBuilder software will change the state of the LTM-10A module from *applicationless* to *unconfigured*. The MIP application will run in the unconfigured state. This means that it will start after this state change has occurred, and the first thing it will do is attempt to synchronize the parallel interface with the host.

If the host is not present, the Neuron Chip's watchdog timer will time out causing periodic resets. These are indicated by flashing the service and reset LEDs on the LTM-10A platform. In this state, the LonBuilder or NodeBuilder software will most likely be unable to communicate with the Neuron Chip, and the load process will halt indicating that it has failed.

Once the MIP application has been successfully loaded and synchronized with the host, the host should send a downlink `niRESYNC` network interface command to the LTM-10A module, and the LTM-10A module will respond with an uplink `niACKSYNC` command. This synchronizes the parallel interface, leaving the write token on the host.

Refer to the *NodeBuilder User's Guide* for more information on developing a LONWORKS host application with the LTM-10A Flash Control Module.

Hardware Interface

The main components of the hardware interface are described in chapter 4 of the *LonBuilder Microprocessor Interface Program (MIP) User's Guide*. The hardware interface for developing a network interface based on the LTM-10A is simplified due to some of the built-in features of the LTM-10A module. For information about ordering LONWORKS documentation, see *Related Documentation* in Chapter 1.

The *host interface* consists of the eight data lines, and three control lines.

The *Uplink Interrupt* can still be optionally used. Since the LTM-10A provides a memory mapped register IRQ output, no special Neuron Chip address decoding is necessary. However an interrupt latch is still needed to allow the host to clear the uplink interrupt state. Note that the ~IRQ output of the LTM-10A is an active low (low going pulse) signal by default. The ~IRQ can be easily changed into an active high signal by modifying the `irq_callback()` function in the MIP_LTM.NC file in the ...\NB\EXA\ directory, as described by the comments in that file.

The *Reset Latch* shown in figure 4-5 of the *LonBuilder Microprocessor Interface Program (MIP) User's Guide* is also needed in order to provide proper synchronization between the LTM-10A module and the host processor whenever the Neuron Chip resets.

Writing a Network Driver

The host network driver that communicates with the parallel port, reset, and interrupt hardware must implement certain functionality for correct operation of the network interface. Once the LTM-10A module has been synchronized with the host, the LTM-10A module will enter the `FLUSH` state. In this state, the LTM-10A module cannot communicate over the network, and cannot send service pin messages. The host network driver should perform any required configuration of the network interface, and then send a `niFLUSH_CANCEL` network interface command to the LTM-10A module to cause it to leave the `FLUSH` state, before the loading process can continue. This process should be performed every time the host detects (via the reset latch) that the LTM-10A module has reset.

Refer to chapter 5 of the *LonBuilder Microprocessor Interface Program (MIP) User's Guide* for information on developing a network driver for the MIP/P50.

Writing a Host Application

Refer to the *LONWORKS Host Application Programmer's Guide* for information on developing your host application.

Example Design

Figure 5.1 is an example of the hardware interface between the LTM-10A Module and a Motorola MC68360 processor.

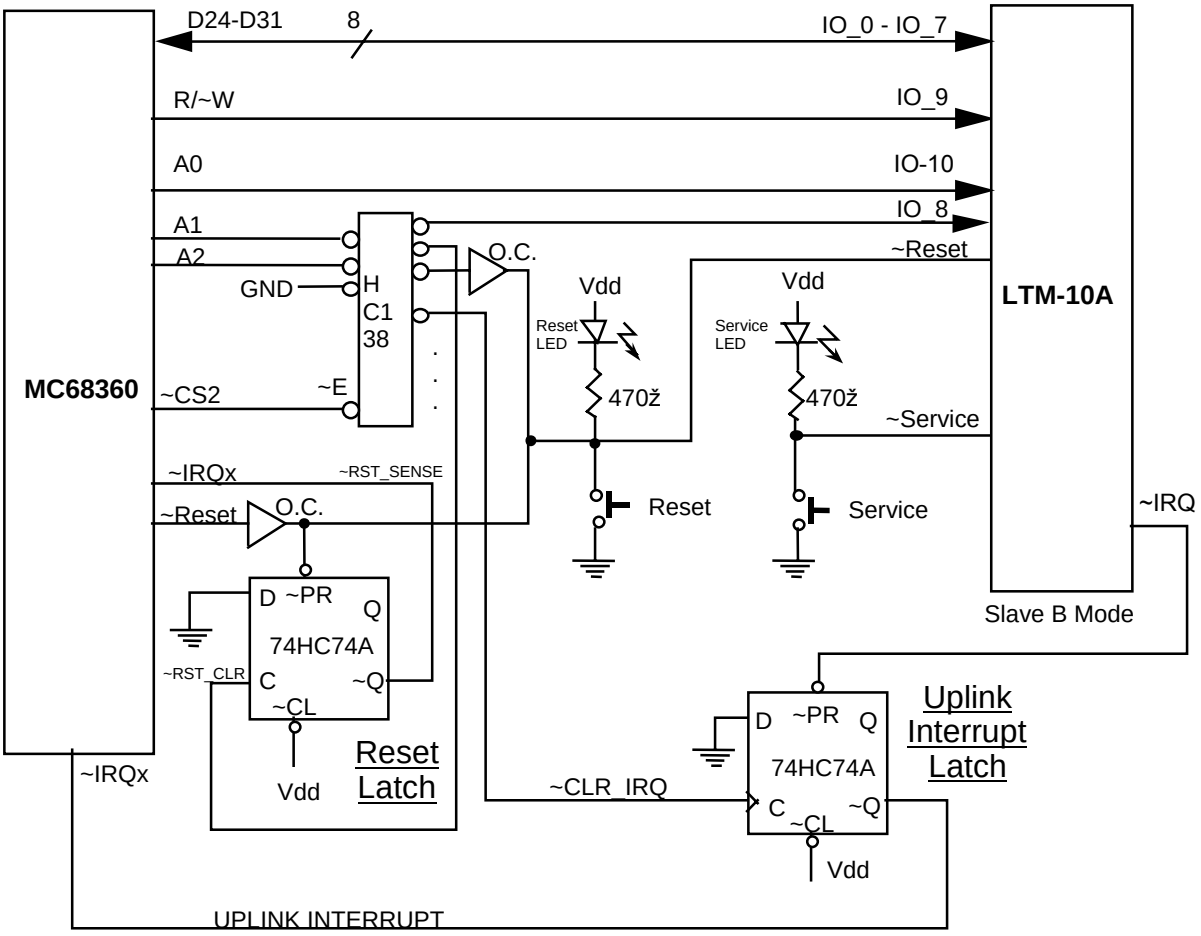


Figure 5.1 MC68360 to LTM-10A Interface